SATELLITE FREE SPACE OPTICS TEST GENERATOR

Petr Tošovský
Doctoral Degree Programme (2), FEEC BUT
E-mail: xtosov00@stud.feec.vutbr.cz

Supervised by: Jiří Šebesta
E-mail: sebestaj@feec.vutbr.cz

ABSTRACT

The presented BER Test Generator was designed as a source of test sequence for Free Space Optics link testing. Transmitted sequence has preset fixed sequence pattern. Bit Error Rate measurement can easy be done by receiving and comparing of the sequence with the known pattern. The BER Test Generator development was constrained to environment conditions on the satellite – ionizing radiation.

1. INTRODUCTION

Free Space Optics (FSO) is relatively a new type of communication. Laser beam as a data carrier is propagated from a source to a target without any extra transmission medium. The transmission medium is an atmosphere or a cosmic environment. It is similar with standard radio transmission. However, the optical signals have very narrow radiation pattern which make the communication jamming-proof and interception-safe (very low signal intensity outside the main beam). Beside of that, high data-rates of data signaling can be used due to nearly unlimited bandwidth.

These advantages are good reason for research of Satellite implementation of this communication [1]. Experimental and even final versions of FSO communication interfaces need to be equipped by a Bit Error Rate measurement (BER) possibility. This type of measurement is provided by transmitting of data sequence. Receiver compares the sequence with error-free pattern of the same sequence. The BER Test Generator is designed as a transmitter of test sequence with variable data-rate. This feature allows the remote change of data-rate which is capable to improve the link power budged of a tested link when it is needed. Due to ionizing radiation environment on the satellite board, technology aspects were considered.

2. IONIZING RADIATION ENVIRONMENT ANALYSIS

Satellite devices are working outside of the Earth atmosphere. This environment is characteristic with the high level of an ionizing radiation. The radiation has typical influence on semiconductors and other electronics components as you can see in [2]. A collision with high energy particle can transfer its energy directly to the semiconductor substrate. This energy portion may significantly change a state of the semiconductor component. Accord-

ing to the type of the radiation, its portion, direction of collision, type of electronics component etc., we can observe different ionizing radiation effects.

Ionizing radiation effects:

- Single-event effect – function violation (depend on LET):
  - Single-Event Upset (SEU) – short-time breakdown
  - Single-Event Latch-up (SEL) – the function of system is stopped
- Total damage
  - Total Ionizing Dose (TID) – device parameter

It is impossible to completely exclude effects of ionizing radiation. The devices should be as simplest as possible or they should provide a runtime self-check function to protect against fatal effects of the radiation. Hence the BER measurement is auxiliary function of FSO transceiver, the BER Test Generator is designed as a simple circuit without any software defined parameters. An eventual SEU can cause temporal malfunction only and SEL produces function interruption (sequence generating is stopped) without persisting damage (current limitation). In the SEL case, the sequence generating is fully recovered after one power cycle. Wherefore, the FSO transceiver Control unit (not a part of the BER Test Generator) is set to periodic power cycling of this device to prevent stable Latch-up effect.

3. BER TEST GENERATOR ARCHITECTURE

The BER Test Generator design was dedicated by a need to have variable data-rate settings and variable data sequence settings. Basic architecture of the BER Test Generator is shown on Fig. 1. Generated sequence has 8 bit length only. This length is quite short (design test); nevertheless it keeps the design simple enough.

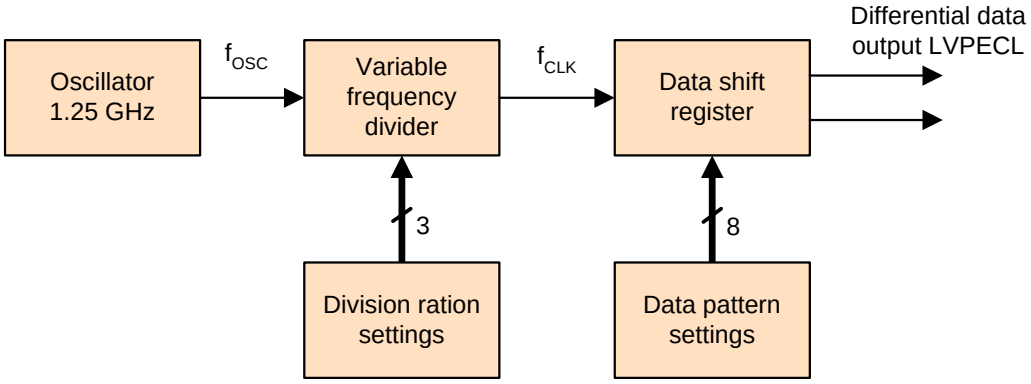

Fig. 1: Block diagram of the BER Test Generator architecture.

Oscillator with 1.25 GHz frequency is a source of f_{OSC} signal for the Variable frequency divider. We can set the division rate of the divider to values 1, 2, 4, 8 or 16. These values equals to the output data-rates of the BER Test Generator 1.25 Gbps, 622, 311, 155 or 78 Mbps. Frequency divided oscillator signal is provided to the data shift register as an input clock signal f_{CLK}. Data shift register automatically latches input data pattern every 8^{th} clock period and transfers one bit of the pattern per one clock period. Output signal is transferred outside the BER Test Generator by high-speed differential logic signaling line.

4. BER TEST GENERATOR REALIZATION

The realization of the BER Test Generator has been done by high-speed ECL logic components. The ECL signaling is transferred between the each part of the Generator via controlled impedance differential microstrip lines – 32 mils thickness with 10 mils gap on 0.38 mm FR4 material with 35µm Cu metallization, gap to other parts at least 40 mils. This type of signaling require appropriate signal termination which is in conformance with required termination type for given signal receiver (Fig. 2.). The Oscillator is represented by FXO-PC736R-1244.160, the Variable frequency divider by SY89874UMI and the Data shift register by MC100EP446FA.

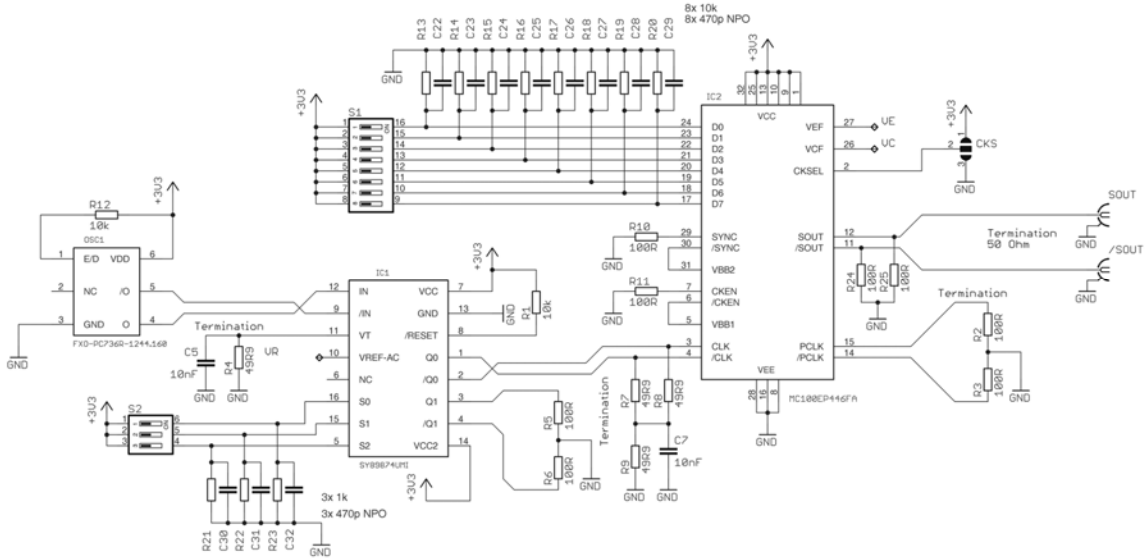

Fig. 2: Schematic diagram of the Test generator.

For laboratory tests, a verification sample of the BER Test Generator was constructed. Impedance controlled transmission lines implementation was proofed. Signal integrity is in good correspondence with calculated expectations.

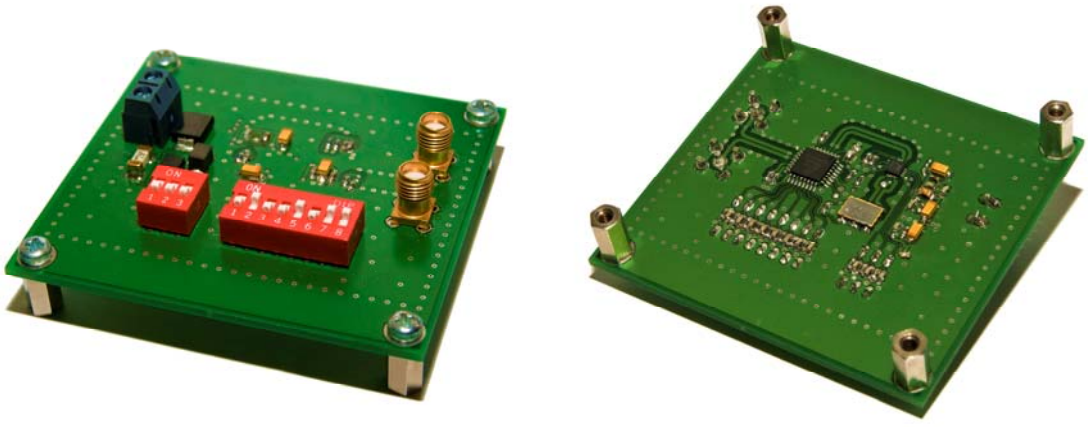

Fig. 3: Function verification sample of the BER Test Generator architecture (laboratory tests).

5. FUNCTION VERIFICATION RESULTS

The generator is able to generate required 8 bit patterns on all data-rates. The output signal has expected parameters for all output data-rates. The BER Test Generator is capable to generate double data-rate by the internal frequency multiplying of its clock signal by 2. The output signal has good signal integrity for 2.5 Gbps data-rate too. However, this data-rate is out of allowed range for the multiplier mode of the output data shift register. Real power consumption is not in correspondence with predicted power consumption. Theoretical power consumption should be 305 mA, typical value less than 250 mA. Typical measured power consumption is about 360 mA. The power consumption can be reduced by DISABLE signal of oscillator – stand-by mode.

Long-term output sequence stability measurement by the Anritsu MP1632C BER tester approved error-free running for 4 hours. Sequence stability of the BER Test Generator for extreme temperature of environment (-50°C to 80°C) is approx. $\Delta f = 27$ kHz.

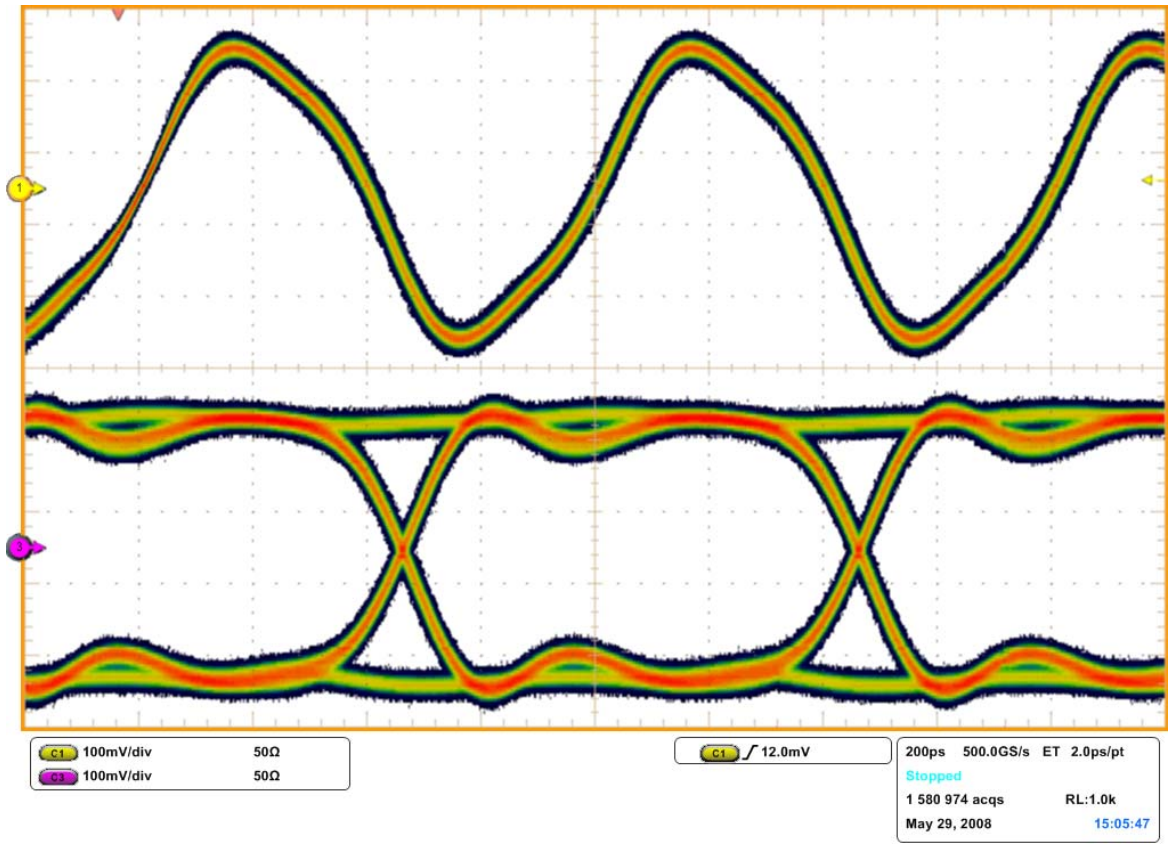

Fig. 4: Recovered clock signal and Eye-diagram of 1.25 Gbps output data sequence signal (Tektronix DPO 7254 scope) on the device output, no link is used.

6. CONCLUSIONS

The designed and constructed BER Test Generator is able to generate the required BER measurement data sequence. Impedance controlled transmission lines guarantee good signal integrity and high noise immunity. The measured stability of output signal is lower than 25 ppm; the value is in conformance with main oscillator parameters (± 20 ppm). Variability of transmission data-rate was checked; standard data-rates 1.25 Gbps, 622 Mbps and 155 Mbps are fully functional. Total power consumption is higher than expected. The increased power consumption is caused by currents to termination circuits. Possible influence of the radiation was discussed and appropriate steps were included to the design. Low complexity of designed circuit should warrant low ionizing radiation sensitivity. Final version of the BER Test Generator can be used not only for testing of FSO links.

The BER Test Generator was embedded to FSO transmitter module and it is under functional tests in present. Future work will be focused to the implementation of the BER Test Generator to a FPGA design. This upgrade of design allows fully pseudo-random test sequence generating with almost arbitrary length. Unfortunately, FPGA has usually SRAM configuration structure what is radiation sensitive structure. Major attention will be concentrated on fail-safe function guarantee.

ACKNOWLEDGEMENTS

Research described in the paper was supported by the Research programs of Brno University of Technology "Electronic Communication Systems and New Generation Technologies (ELKOM)" MSM21630513 and by the Grant Agency of the Czech Republic under contracts "Advanced Methods, Structures, and Components of Electronic Wireless Communication" No. 102/08/H027.

REFERENCES

[1] TOŠOVSKÝ, P.; DORDOVÁ, L. Free Space Optical Channel Parameters Estimation for High Altitude Platform System. In *Proceedings of the 14th Conference on Microwave Techniques COMITE 2008.* Prague: Czechoslovakia Section IEEE, 2008. p. 329-333. ISBN: 978-1-4244-2137-4.

[2] *Space Radiation Effects on Microelectronics* [online]. NASA, 2001 - [cit. 3.3.2009]. http://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf